AMENDMENTS TO THE CLAIMS

Please **ADD** claims 21-29 as shown below. These claims correspond respectively to canceled claims 1-3 and 8-19.

The following is a complete list of all claims in this application.

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Original) A shift register, comprising:

memory devices formed in a shape of an m-row x n-column matrix and shifting data synchronized with a clock signal;

a first switching unit that selectively inverts n-bit data in accordance with a first switching control signal and inputs the inverted data to a first row memory device of each column of said memory devices;

a second switching unit that selectively inverts n-bit data shifted by said memory devices and output to each column of (m)th rows in accordance with a second switching control signal and outputs the inverted data;

a shift comparing unit that outputs a flag signal while outputting a first switching control signal to said first switching unit when data state of the first row memory devices changes, by utilizing n-bit data being input to said first switching unit and output data of the first row memory device included in said memory devices; and

a shift comparing shift register having m-numbers of memory devices arranged in line and that shifts the flag signal output from said shift comparing unit to be synchronized with shift of said memory devices and outputs a second control signal to said second switching unit.

5. (Original) A shift register according to claim 4, wherein said first switching unit and said second switching unit have switching logic corresponding one-to-one to each row of said memory devices, and the switching logic selectively outputs input data and inverted data thereof in accordance with state of the first switching control signal and the second switching control signal.

6. (Original) A shift register according to claim 4, wherein said shift comparing unit comprises:

exclusive OR gates for performing exclusive OR sum of n-bit data to be input to said first switching unit and output data of the first row memory device to said memory device, and outputting the result;

a logical combination unit for logically combining outputs of said exclusive OR gates, and outputting a logic high level as said first switching control signal and a flag signal to be applied to said shift comparing shift register, when a pair of output data and input data of first row memory device is higher than a predetermined number.

7. (Original) A shift register according to claim 6, wherein the number is a number determined by said logical combination unit is larger than half of the number of the first row memory device.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Original) A shift register in a driver circuit of liquid crystal display for driving a liquid crystal panel by generating data, gradation voltage, gate voltage, and column/scan control signals in accordance with an image signal input from an image source, comprising:

memory devices formed in a shape of an m-row x n-column matrix and shifting data synchronized with a clock signal;

a first switching unit that selectively inverts n-bit data in accordance with a first switching control signal and inputs the inverted data to a first row memory device of each column of said memory devices;

a second switching unit that selectively inverts n-bit data shifted by said memory devices and output to each column of (m)th rows in accordance with a second switching control signal and outputs the inverted data;

a shift comparing unit that outputs a flag signal while outputting a first switching control signal to said first switching unit when data state of the first row memory devices changes, by utilizing n-bit data being input to said first switching unit and output data of the first row memory device included in said memory device; and

a shift comparing shift register having m-numbers of memory devices arranged in line and that shifts the flag signal output from said shift comparing unit to be synchronized with shift of said memory devices and outputs a second control signal to said second switching unit.

15. (Original) A shift register according to claim 14, wherein said first switching unit and said second switching unit have switching logic corresponding one-to-one to each row of said memory devices, and the switching logic selectively outputs input data and inverted data thereof in accordance with state of the first switching control signal and the second switching control signal.

16. (Original) A shift register according to claim 14, wherein said shift comparing unit comprises:

exclusive OR gates for performing exclusive OR sum of n-bit data to be input to said first switching unit and output data of the first row memory device to said memory device, and outputting the result;

a logical combination unit for logically combining outputs of said exclusive OR gates, and outputting a logic high level as said first switching control signal and a flag signal to be applied to said shift comparing shift register, when a pair of output data and input data of first row contained in said memory devices is higher than a predetermined number.

17. (Original) A shift register according to claim 16, wherein the number determined by said logical combination unit is larger than half of the number of the first row memory device.

18. (Original) A shift register according to claim 14, wherein the shift register is used in a controller.

19. (Original) A shift register according to claim 14, wherein the shift register is used in column driver ICs.

20. (Original) A shift register according to claim 14, wherein the shift register is used in scan driver ICs.

21. (New) A shift register, comprising:

memory devices formed in a shape of an m row x n column matrix and shifting data synchronized with a clock signal;

a clock signal delay unit for gradually delaying a clock signal applied to said memory devices starting from an (m)th row (n)th column memory device that outputs data, progressing toward a first row of the memory devices where data is inputted;

a data delay unit for delaying the data for a delay time of a clock signal that is applied to an input side of the memory devices; and

a comparing unit to compare data inputted to the first row of memory devices with data outputted from the first row of memory devices, an output from the comparing unit to sequentially delay an operation of each of the memory devices to minimize data conversion and to prevent an instantaneous supply of electric power to multiple memory devices in each m row.

22. (New) A shift register according to claim 21, wherein said clock signal delay unit is configured such that delay portions for delaying the clock signal are one to one matched to (m-1)th row, (m-2)th row, .. 1st row memory devices, and said delay portions output the clock signal with delay time increased in order of (m-1)th row, (m-2)th row, ... 1st row.

23. (New) A shift register according to claim 21, wherein the delay portions output delay time of t, 2t, ... (m-1)t.

24. (New) A driver circuit of liquid crystal display for driving a liquid crystal panel by generating data, gradation voltage, and column/scan control signals in accordance with an image signal input from a predetermined image supply source, the driver circuit having at each unit thereof for processing data, a shift register, the shift register comprising:

memory devices formed in the shape of an m row x n column matrix and shifting data as being synchronized data with a clock signal;

a clock signal delay unit for gradually delaying a clock signal applied to said memory devices starting from an (m)th row (n)th column memory device that outputs data, progressing toward a first row of the memory devices where data is inputted;

a data delay unit for delaying the data for a delay time of a clock signal that is applied to an input side of the memory devices; and

a comparing unit to compare data inputted to the first row of memory devices with data outputted from the first row of memory devices, an output from the comparing unit to sequentially delay an operation of each of the memory devices to minimize data conversion and to prevent an instantaneous supply of electric power to multiple memory devices in each m row.

25. (New) A shift register according to claim 24, wherein said clock signal delay unit is configured such that delay portions for delaying the clock signal are one to one matched to (m-

1)th row, (m-2)th row, ... 1st row memory devices, and said delay portions output the clock signal with delay time increased in order of (m-1)th row, (m-2)the row, ... 1st row.

26. (New) A shift register according to claim 25, wherein the delay portions output delay time of t, 2t, ... (m-1)t.

27. (New) A shift register according to claim 24, wherein the shift register is used in a controller.

28. (New) A shift register according to claim 24, wherein the shift register is used in column driver ICs.

29. (New) A shift register according to claim 24, wherein the shift register is used in scan driver ICs.